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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,304	02/06/2004	Mitsuhiro Yuasa	01165.0912	6472

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EXAMINER	
ASSOUAD, PATRICK J	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,304	YUASA, MITSUHIRO	
	Examiner	Art Unit	
	Patrick J. Assouad	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 June 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5/4/05 & 6/16/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roche et al. (Pub. No. US 2005/0039852 A1) in view of either Miya et al. (US 6,866,744 B2) or Gogol, Jr. et al. (US 5,948,983).

3. Roche et al. disclose :

> There is provided by this invention a wafer probe for measuring plasma and surface characteristics in plasma processing environment that utilizes integrated sensors on a wafer substrate. A microprocessor mounted on the substrate receives input signals from the integrated sensors to process, store, and transmit the data. A wireless communication transceiver receives the data from the microprocessor and transmits information outside of the plasma processing system to a computer that collects the data during plasma processing. The integrated sensors may be dual floating Langmuir probes, temperature measuring devices, resonant beam gas sensors, or hall magnetic sensors. There is also provided a self-contained power source that utilizes the plasma for power that is comprised of a topographically dependent charging device or a charging structure that utilizes stacked capacitors. (abstract)

4. The one-to-one correspondence between the instant claimed invention (independent claim 1) and that of Roche et al. is as follows: a semiconductor fabricating apparatus is the plasma processing system utilized in the semiconductor fabrication

industry of Roche et al.; and the resonant frequency sensor disposed in a processing chamber is disposing the CMOS-based resonant beam sensor of Roche et al. discussed in paras. 0067-0068 (below) into a plasma processing system:

> While thermal sensors, the DFP device and the TDC device have been mentioned in detail here, it is clearly understood by one skilled in the art that the apparatus may include any number of additional sensors. These may include MEMs devices, optical sensor, bulk resistivity devices that are sensitive to rates of etching, curing or deposition or inducement or magnetic fields. In some processes, MEMs devices might be particularly useful sensors in that they are often fashioned from materials that are compatible with plasma-based process environments. One examples of a useful MEMs device is a CMOS-based resonant beam sensor. Such sensors use a micro-machined cantilevered mechanism whose stimulated resonant frequency is dependent upon thermal and mass properties of the beam when exposed to the heat flux of the plasma, gaseous chemical absorbance, or mass changes due to reactive gas etching or deposition.
>
> Some examples of useful MEMs sensor technology include the following devices. A single-chip resonant beam gas sensor as described by Hagleitiner et. al, "A single-chip CMOS Resonant Beam Gas Sensor" 2001 IEEE International Solid-State Circuits Conference, Feb. 6, 2001. This device which was designed to detect the mass absorption of volatile organic compounds could be used in conjunction with present invention to monitor the mass absorption, accumulation or removal as related to a plasma assisted process.

5. The difference between the instant claimed invention (claim 1) and that of Roche et al. lies in the "dermin[ing] the maintenance timing" based on a "change in the resonant frequency of said resonant frequency sensor."

6. Miya et al. disclose:

> A semiconductor processing apparatus for applying plasma treatment to a sample arranged in a vacuum process chamber includes a plasma generator for generating plasma inside the vacuum process chamber and a process gas supply for introducing a process gas into the vacuum process chamber. The apparatus further includes an oscillator for imparting mechanical oscillation to the semiconductor processing apparatus, a receiver for detecting mechanical

oscillation generated by the oscillator in the semiconductor processing apparatus as a signal, and an analyzer for analyzing the detected signal to diagnose whether the vacuum process chamber is normally assembled.

and Gogol, Jr. et al. disclose:

A wall deposit monitoring system for measuring variation in wall deposit thickness in an etch or deposition chamber having a contained reactive environment includes at least one quartz or other piezoelectric crystal sensor installed through a wall of the chamber using a feed-through member. A cover assembly retains the sensor at a projecting end of the feed-through member in a position in proximity with the interior of a chamber wall. The cover includes an opening providing access to the active portion of the sensor for exposure to the reactive environment. An attached oscillating device causes the active portion of the sensor to resonate. As processing is performed in the chamber, a solid reaction product accumulates on the exposed active portion, damping the vibration of the sensor. A detection device sensing the shift in frequency can then calculate the relative change in thickness for a given material. When used with highly reactive environments, the assembly is constructed of non-reactive materials which are sufficiently electrical and thermally conductive.

7. And both Miyal et al. and Gogol, Jr. et al. teach the difference (indicated above) in at least the following passages:

from Miyal et al., (cols. 11-12):

Next, the digital data is transferred to estimation/diagnosis means 41. The estimation/diagnosis means 41 compares the digital data with the threshold value stored in the database or with the past history data and diagnoses whether or not the semiconductor processing apparatus is now under the normal condition. To make this diagnosis, whether or not the digital data exceeds a predetermined threshold value or its range is judged, for example. Comparison with the history data under the normal condition may be used, too. Furthermore, the shift of the change from a plurality of past history data is determined and judgment may be made on the basis of this shift. The estimation/diagnosis means 41 can diagnose whether or not the semiconductor processing apparatus is now under the normal condition and can also conduct estimation. In other words, the estimation/diagnosis means 41 analyzes the shift of the past history data stored in the database, and can estimate that the subsequent wet cleaning should be carried out after how many hours, or can

estimate after how many hours constituent components inside the process chamber reach their service life (Step S5).

Next, the diagnostic result is transferred to a computer 42 for controlling the semiconductor processing apparatus. The semiconductor processing apparatus controlling computer 42 continues processing when the diagnostic result is normal (Step S6), and stops the processing and raises an alarm when the diagnostic result proves abnormal (Steps S7 and S8).

When the estimation result of the estimation/diagnosis means indicates the wet cleaning timing or the life of the constituent components, the process is continued as such and alarm means raises an alarm (Steps S6 and S8).

and from Gogol, Jr. et al., col. 2, lines 57-67:

An advantage of the present invention is that the wall deposit thickness of a deposition or etch chamber can be easily monitored, thereby reducing the frequency of opening the chamber to interrupt in-process activity.

A further advantage of the present invention is that an accumulated threshold wall deposit thickness value or limit for cleaning or other purposes can be selected, by which the described monitoring system can automatically inform the user when this threshold limit has been reached, despite variations in processing conditions or other extraneous factors.

8. Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the maintenance timing teachings of either Miyal et al. or Gogol, Jr. et al. into the plasma processing measurement apparatus of Roche et al. because Roche et al. knew that:

Spatial and temporal variation in plasma characteristics and the work piece surface temperature can strongly influence the performance and yield of plasma-based processes, such as those encountered in semiconductor manufacture. In such processes, variations in physical plasma parameters that occur adjacent to the process work piece directly impact process metrics which may include the following: (1) etch rates and etch profile control, (2) surface charging effects and device or film damage, and (3) thin film deposition rates, density,

> coverage, morphology, stress and adhesion. Some common plasma parameters that drive surface processes on a work piece, such as a semiconductor substrate wafer, include charged-particle density and flux (ion and electron density), apparent electron temperature, ion energies, neutral gas temperature, density and flux of reactive gas species, and plasma radiative emissions. It is also known that surface temperature of the work piece or wafer can play a very critical role in many of the surface reactions and results of the plasma process. (Background/Brief Description of the Prior art of Roche et al.)

and performing required maintenance of a plasma-based semiconductor manufacturing apparatus provides enhances quality control to avoid extremes in final product variations.

9. As per dependent claim 2 which relates to a "micro machine", see at least the aforementioned discussion of MEMS devices or "micro machined cantilevered mechanisms" of Roche et al. in paras. 0067-0068.

10. As per dependent claim 3 which relates to etching or deposition and chamber condition, see at least the aforementioned Background/Brief Description of the Prior art of Roche et al., and as to the claimed "database", see at least the aforementioned database of Miya et al. (cols. 11-12, reproduced above).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See the attached PTO-892.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick J. Assouad whose telephone number is 571-272-2210. The examiner can normally be reached on Tuesday-Friday, 6:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patrick J Assouad
Primary Examiner
Art Unit 2857

pja